Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.07 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.08 secs

--> Reading design: WS.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Parsing

3) HDL Elaboration

4) HDL Synthesis

4.1) HDL Synthesis Report

5) Advanced HDL Synthesis

5.1) Advanced HDL Synthesis Report

6) Low Level Synthesis

7) Partition Report

8) Design Summary

8.1) Primitive and Black Box Usage

8.2) Device utilization summary

8.3) Partition Resource Summary

8.4) Timing Report

8.4.1) Clock Information

8.4.2) Asynchronous Control Signals Information

8.4.3) Timing Summary

8.4.4) Timing Details

8.4.5) Cross Clock Domains Report

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "WS.prj"

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "WS"

Output Format : NGC

Target Device : xa7a100t-2I-csg324

---- Source Options

Top Module Name : WS

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 32

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Parsing \*

=========================================================================

Parsing VHDL file "D:\Users\final\seg7.vhd" into library work

Parsing entity <seg7>.

Parsing architecture <Behavioral> of entity <seg7>.

Parsing VHDL file "D:\Users\final\WS.vhd" into library work

Parsing entity <WS>.

Parsing architecture <fsm> of entity <ws>.

=========================================================================

\* HDL Elaboration \*

=========================================================================

Elaborating entity <WS> (architecture <fsm>) from library <work>.

Elaborating entity <seg7> (architecture <Behavioral>) from library <work>.

INFO:HDLCompiler:679 - "D:\Users\final\WS.vhd" Line 77. Case statement is complete. others clause is never selected

=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <WS>.

Related source file is "D:\Users\final\WS.vhd".

WARNING:Xst:737 - Found 1-bit latch for signal <ps>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

Found 3-bit comparator lessequal for signal <n0002> created at line 56

Found 3-bit comparator lessequal for signal <n0006> created at line 59

Found 3-bit comparator lessequal for signal <n0014> created at line 67

Found 3-bit comparator lessequal for signal <n0016> created at line 70

Summary:

inferred 1 Latch(s).

inferred 4 Comparator(s).

inferred 10 Multiplexer(s).

Unit <WS> synthesized.

Synthesizing Unit <seg7>.

Related source file is "D:\Users\final\seg7.vhd".

Summary:

no macro.

Unit <seg7> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Latches : 1

1-bit latch : 1

# Comparators : 4

3-bit comparator lessequal : 4

# Multiplexers : 10

1-bit 2-to-1 multiplexer : 7

2-bit 2-to-1 multiplexer : 3

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

WARNING:Xst - The specified part-type was not generated at build time. XST is loading the full part-type and will therefore consume more CPU and memory.

Loading device for application Rf\_Device from file '7a100t.nph' in environment C:\Xilinx\14.7\ISE\_DS\ISE\.

Loading device for application Rf\_Device from file '7a100t.nph' in environment C:\Xilinx\14.7\ISE\_DS\ISE\.

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Comparators : 4

3-bit comparator lessequal : 4

# Multiplexers : 10

1-bit 2-to-1 multiplexer : 7

2-bit 2-to-1 multiplexer : 3

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <WS> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block WS, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Found no macro

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : WS.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 4

# GND : 1

# LUT6 : 2

# VCC : 1

# FlipFlops/Latches : 1

# LDC : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 20

# IBUF : 6

# OBUF : 14

Device utilization summary:

---------------------------

Selected Device : xa7a100tcsg324-2i

Slice Logic Utilization:

Number of Slice Registers: 1 out of 126800 0%

Number of Slice LUTs: 2 out of 63400 0%

Number used as Logic: 2 out of 63400 0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 3

Number with an unused Flip Flop: 2 out of 3 66%

Number with an unused LUT: 1 out of 3 33%

Number of fully used LUT-FF pairs: 0 out of 3 0%

Number of unique control sets: 1

IO Utilization:

Number of IOs: 21

Number of bonded IOBs: 21 out of 210 10%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clock | BUFGP | 1 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -2

Minimum period: 0.936ns (Maximum Frequency: 1068.319MHz)

Minimum input arrival time before clock: 0.863ns

Maximum output required time after clock: 1.553ns

Maximum combinational path delay: 1.219ns

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clock'

Clock period: 0.936ns (frequency: 1068.319MHz)

Total number of paths / destination ports: 1 / 1

-------------------------------------------------------------------------

Delay: 0.936ns (Levels of Logic = 1)

Source: ps (LATCH)

Destination: ps (LATCH)

Source Clock: clock falling

Destination Clock: clock falling

Data Path: ps to ps

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

LDC:G->Q 3 0.472 0.367 ps (ps)

LUT6:I5->O 1 0.097 0.000 S<0>1 (S<0>)

LDC:D -0.028 ps

----------------------------------------

Total 0.936ns (0.569ns logic, 0.367ns route)

(60.8% logic, 39.2% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clock'

Total number of paths / destination ports: 6 / 2

-------------------------------------------------------------------------

Offset: 0.863ns (Levels of Logic = 2)

Source: moist<2> (PAD)

Destination: ps (LATCH)

Destination Clock: clock falling

Data Path: moist<2> to ps

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 3 0.001 0.765 moist\_2\_IBUF (moistOut\_2\_OBUF)

LUT6:I0->O 1 0.097 0.000 S<0>1 (S<0>)

LDC:D -0.028 ps

----------------------------------------

Total 0.863ns (0.098ns logic, 0.765ns route)

(11.4% logic, 88.6% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clock'

Total number of paths / destination ports: 5 / 5

-------------------------------------------------------------------------

Offset: 1.553ns (Levels of Logic = 2)

Source: ps (LATCH)

Destination: mySeg<5> (PAD)

Source Clock: clock falling

Data Path: ps to mySeg<5>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

LDC:G->Q 3 0.472 0.628 ps (ps)

LUT6:I2->O 4 0.097 0.356 sev/\_n00071 (mySeg\_1\_OBUF)

OBUF:I->O 0.000 mySeg\_5\_OBUF (mySeg<5>)

----------------------------------------

Total 1.553ns (0.569ns logic, 0.984ns route)

(36.6% logic, 63.4% route)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 25 / 9

-------------------------------------------------------------------------

Delay: 1.219ns (Levels of Logic = 3)

Source: light (PAD)

Destination: mySeg<5> (PAD)

Data Path: light to mySeg<5>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 3 0.001 0.765 light\_IBUF (lightOut\_OBUF)

LUT6:I0->O 4 0.097 0.356 sev/\_n00071 (mySeg\_1\_OBUF)

OBUF:I->O 0.000 mySeg\_5\_OBUF (mySeg<5>)

----------------------------------------

Total 1.219ns (0.098ns logic, 1.121ns route)

(8.0% logic, 92.0% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

Clock to Setup on destination clock clock

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clock | | | 0.936| |

---------------+---------+---------+---------+---------+

=========================================================================

Total REAL time to Xst completion: 23.00 secs

Total CPU time to Xst completion: 22.92 secs

-->

Total memory usage is 4948068 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 2 ( 0 filtered)

Number of infos : 0 ( 0 filtered)